FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11123-1E

MEMORY

Un-buffered

4 M × 64 BIT SYNCHRONOUS DYNAMIC RAM SO-DIMM

MB8504S064AE-100/-84/-67/-100L/-84L/-67L

144-pin, 2 Clock, 1-bank, based on 4 M × 16 Bit SDRAMs with SPD

■ DESCRIPTION

The Fujitsu MB8504S064AE is a fully decoded, CMOS Synchronous Dynamic Random Access Memory (SDRAM) Module consisting of four MB811641642A devices which organized as two banks of 4 M × 16 bits and a 2K-bit serial EEPROM on a 144-pin glass-epoxy substrate.

The MB8504S064AE features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence.

The MB8504S064AE is optimized for those applications requiring high speed, high performance and large memory storage, and high density memory organizations.
This module is ideally suited for workstations, PCs, laser printers, and other applications where a simple interface is needed.

■ PRODUCT LINE & FEATURES

Parameter		MB8504S064AE-100/100L	MB8504S064AE-84/84L	MB8504S064AE-67/67L
Clock Frequency		100 MHz max.	84 MHz max.	67 MHz max.
Burst Mode Cycle Time		10 ns max. (CL = 3) 15 ns max. (CL = 2)	12 ns max. (CL = 3) 17 ns max. (CL = 2)	15 ns max. (CL = 3) 20 ns max. (CL = 2)
$\overline{RAS}$ Access Time		54 ns max.	56 ns max.	60 ns max.
$\overline{CAS}$ Access Time		24 ns max.	26 ns max.	30 ns max.
Output Valid from Clock		8.5 ns max. (CL = 3) 9 ns max. (CL = 2)	8.5 ns max. (CL = 3) 10 ns max. (CL = 2)	9 ns max. (CL = 3) 10 ns max. (CL = 2)
Power Dissipation	Burst Mode	2160 mW max.	1872 mW max.	1440 mW max.
	Power Down Mode	43.2 mW max.(std. power) 14.4 mW max.(low power)		

- Unbuffered 144-pin SO-DIMM Socket Type (Lead pitch: 0.8 mm)
- Conformed to JEDEC Standard (2 CLK)
- Organization: 4,194,304 words × 64 bits
- Memory: MB811641642A (1 M × 16, 4-bank) × 4 pcs.
- 3.3 V ±0.3 V Supply Voltage
- All input/output LVTTL compatible
- 4096 Refresh Cycle every 65.6 ms
- Auto and Self Refresh
- CKE Power Down Mode
- DQM Byte Masking (Read/Write)
- Serial Presence Detect (SPD) with Serial EEPROM
- Module size:
  1.0” (height) × 2.66” (length) × 0.15” (thickness)

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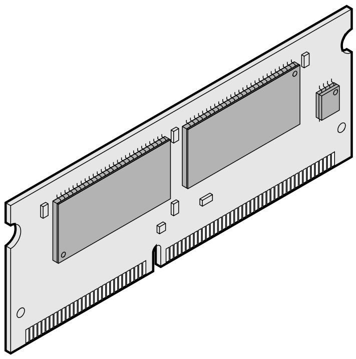
■ PACKAGE

144-pin plastic DIMM (socket type)



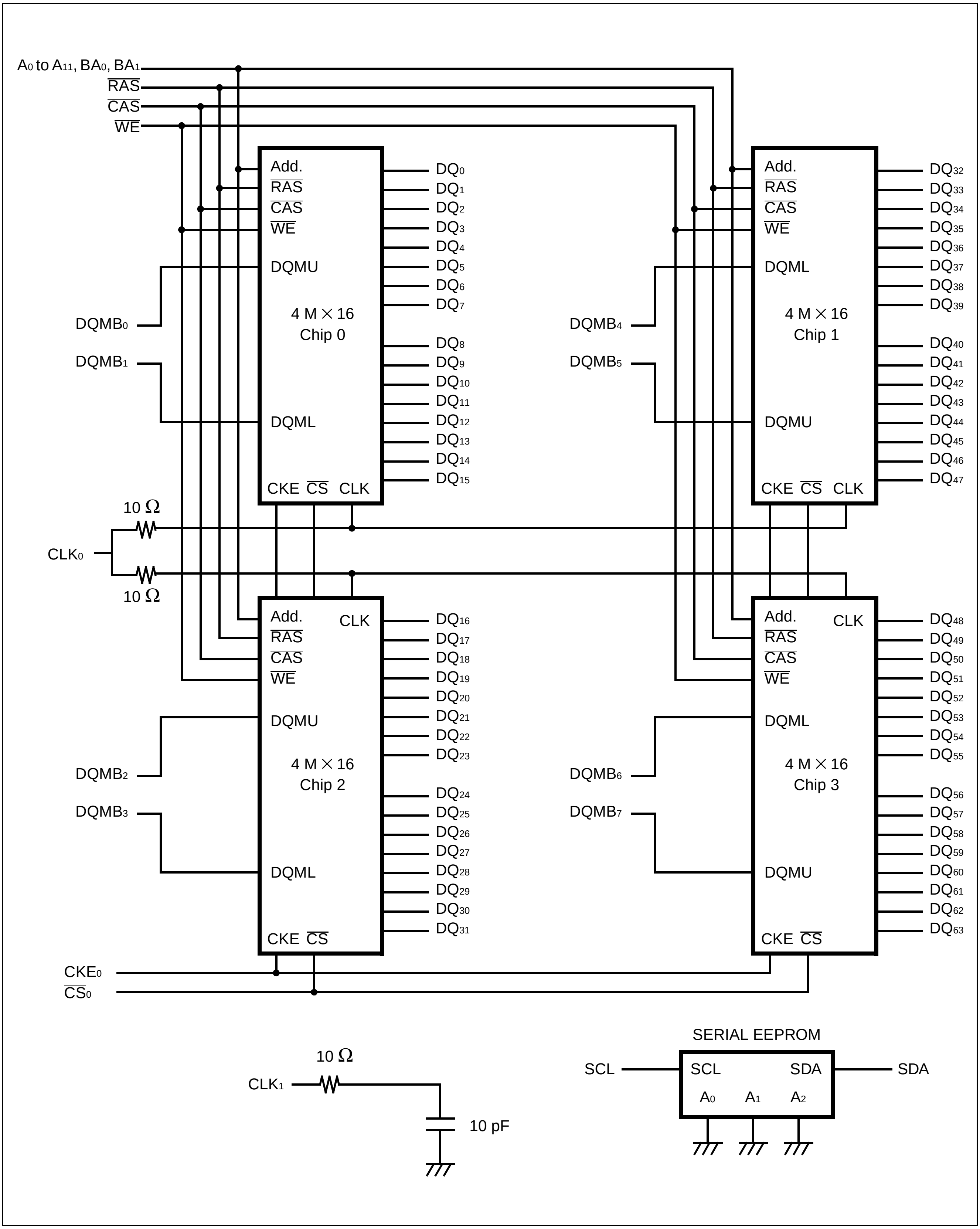
(MDS-144P-P08)

Package and Ordering Information

– 144-pin SO-DIMM, order as MB8504S064AE-××DG (DG = Gold Pad)

MB8504S064AE-100/-84/-67/-100L/-84L/-67L

■ BLOCK DIAGRAM



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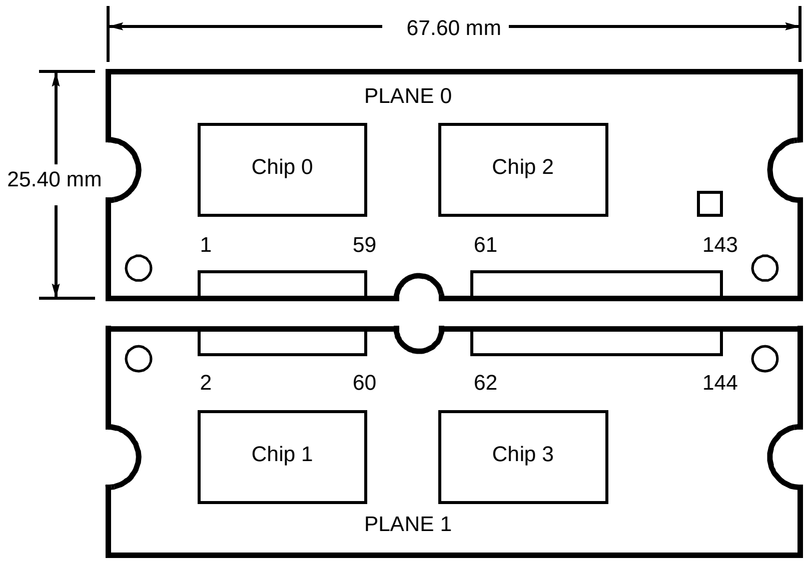
■ PIN ASSIGNMENTS

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V_{SS}	49	DQ_{13}	97	DQ_{22}	2	V_{SS}	50	DQ_{45}	98	DQ_{54}
3	DQ_0	51	DQ_{14}	99	DQ_{23}	4	DQ_{32}	52	DQ_{46}	100	DQ_{55}
5	DQ_1	53	DQ_{15}	101	V_{CC}	6	DQ_{33}	54	DQ_{47}	102	V_{CC}
7	DQ_2	55	V_{SS}	103	A_6	8	DQ_{34}	56	V_{SS}	104	A_7
9	DQ_3	57	N.C.	105	A_8	10	DQ_{35}	58	N.C.	106	BA_0
11	V_{CC}	59	N.C.	107	V_{SS}	12	V_{CC}	60	N.C.	108	V_{SS}
13	DQ_4	61	CLK_0	109	A_9	14	DQ_{36}	62	CKE_0	110	BA_1
15	DQ_5	63	V_{CC}	111	A_{10}	16	DQ_{37}	64	V_{CC}	112	A_{11}
17	DQ_6	65	$\overline{RAS}$	113	V_{CC}	18	DQ_{38}	66	$\overline{CAS}$	114	V_{CC}
19	DQ_7	67	$\overline{WE}$	115	$DQMB_2$	20	DQ_{39}	68	N.C.	116	$DQMB_6$
21	V_{SS}	69	$\overline{CS}_0$	117	$DQMB_3$	22	V_{SS}	70	N.C.	118	$DQMB_7$
23	$DQMB_0$	71	N.C.	119	V_{SS}	24	$DQMB_4$	72	N.C.	120	V_{SS}
25	$DQMB_1$	73	N.C.	121	DQ_{24}	26	$DQMB_5$	74	CLK_1	122	DQ_{56}
27	V_{CC}	75	V_{SS}	123	DQ_{25}	28	V_{CC}	76	V_{SS}	124	DQ_{57}
29	A_0	77	N.C.	125	DQ_{26}	30	A_3	78	N.C.	126	DQ_{58}
31	A_1	79	N.C.	127	DQ_{27}	32	A_4	80	N.C.	128	DQ_{59}
33	A_2	81	V_{CC}	129	V_{CC}	34	A_5	82	V_{CC}	130	V_{CC}
35	V_{SS}	83	DQ_{16}	131	DQ_{28}	36	V_{SS}	84	DQ_{48}	132	DQ_{60}
37	DQ_8	85	DQ_{17}	133	DQ_{29}	38	DQ_{40}	86	DQ_{49}	134	DQ_{61}
39	DQ_9	87	DQ_{18}	135	DQ_{30}	40	DQ_{41}	88	DQ_{50}	136	DQ_{62}
41	DQ_{10}	89	DQ_{19}	137	DQ_{31}	42	DQ_{42}	90	DQ_{51}	138	DQ_{63}
43	DQ_{11}	91	V_{SS}	139	V_{SS}	44	DQ_{43}	92	V_{SS}	140	V_{SS}
45	V_{CC}	93	DQ_{20}	141	SDA	46	V_{CC}	94	DQ_{52}	142	SCL
47	DQ_{12}	95	DQ_{21}	143	V_{CC}	48	DQ_{44}	96	DQ_{53}	144	V_{CC}

TOP VIEW



(MDS-144P-P08)

■ PIN DESCRIPTIONS

Symbol	I/O	Function	Symbol	I/O	Function
A_0 to A_{11}	I	Address Input	$\overline{CS_0}$	I	Chip Select
BA_0, BA_1	I	Bank Address	DQ_0 to DQ_{63}	I/O	Data Input/Data Output
$\overline{RAS}$	I	Row Address Strobe	V_{CC}	—	Power Supply (+3.3 V)
$\overline{CAS}$	I	Column Address Strobe	V_{SS}	—	Ground (0 V)
$\overline{WE}$	I	Write Enable	N.C.	—	No Connection
$DQMB_0$ to $DQMB_7$	I	Data (DQ) Mask	SCL	I	Serial PD Clock
CLK_0, CLK_1	I	Clock Input	SDA	I/O	Serial PD Address/Data Input/Output
CKE_0	I	Clock Enable			

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■ SERIAL-PD INFORMATION

Byte	Function Described		Hex Value		
			-100/100L	-84/84L	-67/67L
0	Defines Number of Bytes Written into Serial Memory at Module Manufacture	128 Byte	80h	80h	80h
1	Total Number of Bytes of SPD Memory Device	256 Byte	08h	08h	08h
2	Fundamental Memory Type	SDRAM	04h	04h	04h
3	Number of Row Addresses	12	0Ch	0Ch	0Ch
4	Number of Column Addresses	8	08h	08h	08h
5	Number of Module Banks	1 bank	01h	01h	01h
6	Data Width	64 bit	40h	40h	40h
7	Data Width (Continuation)	+0	00h	00h	00h
8	Interface Type	LVTTL	01h	01h	01h
9	SDRAM Cycle Time (Highest CAS Latency)	10/12/15 ns	A0h	C0h	F0h
10	SDRAM Access from Clock (Highest CAS Latency)	8.5/8.5/9 ns	85h	85h	90h
11	DIMM Configuration Type	Non-Parity	00h	00h	00h
12	Refresh Rate/Type	Self, Normal	80h	80h	80h
13	Primary SDRAM Width	×16	10h	10h	10h
14	Error Checking SDRAM Width	0	00h	00h	00h
15	Minimum Clock Delay for Back to Back Random Column Addresses	1 Cycle	01h	01h	01h
16	Burst Lengths Supported	1, 2, 4, 8, Page	8Fh	8Fh	8Fh
17	Number of Banks on Each SDRAM Device	4 bank	04h	04h	04h
18	CAS Latency	2, 3	06h	06h	06h
19	CS Latency	0	01h	01h	01h
20	Write Latency	0	01h	01h	01h
21	SDRAM Module Attributes	UN-buffer	00h	00h	00h
22	SDRAM Device Attributes	*1	06h	06h	06h
23	SDRAM Cycle Time (2nd. Highest CAS Latency)	15/17/20 ns	F0h	20h	FFh
24	SDRAM Access from Clock (2nd. Highest CAS Latency)	9/10/10 ns	90h	A0h	A0h
25	SDRAM Cycle Time (3rd. Highest CAS Latency)	No Support	00h	00h	00h
26	SDRAM Access from Clock (3rd. Highest CAS Latency)	No Support	00h	00h	00h
27	Precharge to Activate Min. (t_{RP})	30/35/40 ns	1Eh	23h	28h
28	Row Activate to Row Activate Min. (t_{RRD})	30/30/30 ns	1Eh	1Eh	1Eh
29	$\overline{RAS}$ to $\overline{CAS}$ Delay Min. (t_{RCD})	30/30/30 ns	1Eh	1Eh	1Eh
30	Activate to Precharge Minimum Time (t_{RAS})	60/65/70 ns	3Ch	41h	46h
31	Module Bank Density	32 MByte	08h	08h	08h
32 to 61	Unused Storage Locations	—	00h	00h	00h
62	SPD Data Revision Code	1	01h	01h	01h
63	Checksum for Byte 0 to 62	*2	58h	C2h	E6h
64 to 98	Manufacturer's Information: Unused Storage	—	00h	00h	00h
99 to 127	Vendor Specific Data: Unused Storage	—	00h	00h	00h
128+	Unused Storage Locations	—	—	—	—

Note: Any write operation must NOT be executed into the addresses of Byte 0 to Byte 127.
Some or all data stored into Byte 0 to Byte 127 may be broken.

*1. SDRAM Device Attributes

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBD	TBD	Upper V_{CC} tolerance 0 = 10%	Lower V_{CC} tolerance 0 = 10%	Supports Write 1/ Read Burst	Supports Precharge All	Supports Auto-Precharge	Supports Early $\overline{RAS}$ Precharge
0	0	0	0	0	1	1	0

*2. Checksum for Bytes 0 to 62

This byte is the checksum for bytes 0 through 62. This byte contains the value of the low 8-bits of the arithmetic sum of bytes 0 through 62.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Supply Voltage*	V_{CC}	–0.5	+4.6	V
Input Voltage*	V_{IN}	–0.5	+4.6	V
Output Voltage*	V_{OUT}	–0.5	+4.6	V
Storage Temperature	T_{STG}	–55	+125	°C
Power Dissipation	P_D	—	4.0	W
Output Current (D.C.)	I_{OUT}	–50	+50	mA

* : Voltages referenced to V_{SS} (= 0 V)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	*1	V_{CC}	3.0	3.3	3.6	V
		V_{SS}	0	0	0	V
Input High Voltage, All Inputs	*1	V_{IH}	2.0	—	V_{CC} +0.5	V
Input Low Voltage, All Inputs	*1, 2	V_{IL}	–0.5	—	0.8	V
Ambient Temperature		T_A	0	—	+70	°C

*1. Voltages referenced to V_{SS} (= 0 V)
*2. V_{IL} (min) = –1.5 V AC (Pulse Width ≤ 5 ns)

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device’s electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

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■ CAPACITANCE

(V_{CC} = +3.3 V, f = 1 MHz, T_A = +25°C)

Parameter		Symbol	Value		Unit
			Min.	Max.	
Input Capacitance	A_0 to A_{11}, BA_0, BA_1	C_{IN1}	—	30	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	30	pF
	$\overline{CS_0}$	C_{IN3}	—	26	pF
	CKE_0	C_{IN4}	—	26	pF
	CLK_0, CLK_1	C_{IN5}	—	30	pF
	$DQMB_0$ to $DQMB_7$	C_{IN6}	—	12	pF
	SCL	C_{SCL}	—	7	pF
Input/Output Capacitance	SDA	C_{SDA}	—	7	pF
	DQ_0 to DQ_{63}	C_{DQ}	—	13	pF

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■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes		Symbol	Condition	Value Min.	Max. Std. ver.	Max. Low ver.	Unit
Operating Current (Average Power Supply Current)	*1	-100/100L	I_{CC1S}	No Burst; t_{CK} = min t_{RC} = min One Bank Active 0 V ≤ V_{IN} ≤ V_{CC}	—	320		mA
		-84/84L				300		mA
		-67/67L				280		mA
		-100/100L	I_{CC1D}	No Burst; t_{CK} = min t_{RC} = min Two Banks Active 0 V ≤ V_{IN} ≤ V_{CC}	—	560		mA
		-84/84L				520		mA
		-67/67L				480		mA
Precharge Standby Current (Power Supply Current)	*1		I_{CC2P}	CKE = V_{IL}, t_{CK} = min All Banks Idle 0 V ≤ V_{IN} ≤ V_{CC}	—	12	4	mA
			I_{CC2PS}	CKE = V_{IL}, CLK = V_{IL} All Banks Idle 0 V ≤ V_{IN} ≤ V_{CC}	—	8	1	mA
			I_{CC2N}	CKE = V_{IH}, t_{CK} = min All Banks Idle 0 V ≤ V_{IN} ≤ V_{CC}	—	80		mA
			I_{CC2NS}	CKE = V_{IH}, CLK = V_{IL} All Banks Idle 0 V ≤ V_{IN} ≤ V_{CC}	—	20		mA
Active Standby Current (Power Supply Current)	*1		I_{CC3P}	CKE = V_{IL}, t_{CK} = min Any Bank Active 0 V ≤ V_{IN} ≤ V_{CC}	—	20	12	mA
			I_{CC3PS}	CKE = V_{IL}, CLK = V_{IL} Any Bank Active 0 V ≤ V_{IN} ≤ V_{CC}	—	16	8	mA
			I_{CC3N}	CKE = V_{IH}, t_{CK} = min Any Bank Active 0 V ≤ V_{IN} ≤ V_{CC}	—	100		mA
			I_{CC3NS}	CKE = V_{IH}, CLK = V_{IL} Any Bank Active 0 V ≤ V_{IN} ≤ V_{CC}	—	40		mA
Burst Mode Current (Average Power Supply Current)	*1	-100/100L	I_{CC4}	t_{CK} = min 0 V ≤ V_{IN} ≤ V_{CC}	—	600		mA
		-84/84L			—	520		mA
		-67/67L			—	400		mA
Auto-refresh Current (Average Power Supply Current)	*1	-100/100L	I_{CC5}	Auto Refresh t_{CK} = min t_{RC} = min 0 V ≤ V_{IN} ≤ V_{CC}	—	720		mA
		-84/84L			—	660		mA
		-67/67L			—	600		mA

(Continued)

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(Continued)

Parameter	Notes	Symbol	Condition	Value			Unit
				Min.	Max.		
					Std. ver.	Low ver.	
Self-refresh Current (Average Power Supply Current)		I_{CC6}	CKE = V_{IL}, 0 V ≤ V_{IN} ≤ V_{CC}	—	8	2	mA
Input Leakage Current (All Inputs)		$I_{I(L)}$	0 V ≤ V_{IN} ≤ V_{CC} All other pins not under test = 0 V	–30	30		µA
Output Leakage Current		$I_{O(L)}$	Output is disabled (Hi-Z) 0 V ≤ V_{IN} ≤ V_{CC}	–10	10		µA
LVTTL Output High Voltage	*2	V_{OH}	I_{OH} = –2.0 mA	2.4	—		V
LVTTL Output Low Voltage	*2	V_{OL}	I_{OL} = +2.0 mA	—	0.4		V

Notes: *1. I_{CC} depends on the output termination, load conditions, clock cycle rate and signal clock rate. The specified values are obtained with the output open and no termination register.
*2. Voltages referenced to V_{SS} (= 0 V)
*3. An initial pause (DESL on NOP) of 200 µs is required after power-on followed by a minimum of eight Auto-refresh cycles.
*4. DC characteristics is the Serial PD standby state (V_{IN} = GND or V_{CC}).

■ AC CHARACTERISTICS

(1) BASE CHARACTERISTICS
(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Notes	Symbol	MB8504S064AE -100/100L		MB8504S064AE -84/84L		MB8504S064AE -67/67L		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
1	Clock Period	CL = 3	t_{CK}	10	—	12	—	15	—	ns
		CL = 2		15	—	17	—	20	—	ns
2	Clock High Time		t_{CH}	3.5	—	4	—	4	—	ns
3	Clock Low Time		t_{CL}	3.5	—	4	—	4	—	ns
4	Input Setup Time		t_{SI}	3	—	3	—	3	—	ns
5	Input Hold Time		t_{HI}	1	—	1	—	1	—	ns
6	Output Valid from Clock (t_{CLK} = min) *1, *2	CL = 3	t_{AC}	—	8.5	—	8.5	—	9	ns
		CL = 2		—	9	—	10	—	10	
7	Output in Low-Z		t_{LZ}	3	—	3	—	3	—	ns
8	Output in High-Z *3	CL = 3	t_{HZ}	3	8.5	3	8.5	3	9	ns
		CL = 2		3	9	3	10	3	10	ns
9	Output Hold Time		t_{OH}	3	—	3	—	3	—	ns
10	Time between Refresh		t_{REF}	—	65.6	—	65.6	—	65.6	ms
11	Transition Time		t_T	0.5	2	0.5	2	0.5	2	ns
12	Power Down Exit Time		t_{PDE}	3	—	4	—	5	—	ns

(2) BASE VALUES FOR CLOCK COUNT/LATENCY

No.	Parameter	Notes	Symbol	MB8504S064AE -100/100L		MB8504S064AE -84/84L		MB8504S064AE -67/67L		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
1	$\overline{\text{RAS}}$ Cycle Time	*4	t_{RC}	90	—	100	—	110	—	ns
2	$\overline{\text{RAS}}$ Access Time	*5	t_{RAC}	—	54	—	56	—	60	ns
3	$\overline{\text{CAS}}$ Access Time	*6, *9	t_{CAC}	—	24	—	26	—	30	ns
4	$\overline{\text{RAS}}$ Precharge Time		t_{RP}	30	—	35	—	40	—	ns
5	$\overline{\text{RAS}}$ Active Time		t_{RAS}	60	100000	65	100000	70	100000	ns
6	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	*7	t_{RCD}	30	—	30	—	30	—	ns
7	Write Recovery Time		t_{WR}	10	—	12	—	15	—	ns
8	Write to Precharge Read Delay Time		t_{RWL}	10	—	12	—	15	—	ns
9	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Bank Active Delay Time		t_{RRD}	20	—	20	—	20	—	ns

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(3) CLOCK COUNT FORMULA (*8)

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}}$$ (Round off a whole number)

(4) LATENCY (The latency values on these parameters are fixed regardless of clock period.)

No.	Parameter		Symbol	MB8504S064AE -100/100L	MB8504S064AE -84/84L	MB8504S064AE -67/67L	Unit
1	CKE to Clock Disable		l_{CKE}	1	1	1	Cycle
2	DQM to Output in High-Z		l_{DQZ}	2	2	2	Cycle
3	DQM to Input Data Delay		l_{DQD}	0	0	0	Cycle
4	Last Output to Write Command Delay		l_{OWD}	2	2	2	Cycle
5	Write Command to Input Data Delay		l_{DWD}	0	0	0	Cycle
6	Precharge to Output in High-Z Delay	CL = 3	l_{ROH}	3	3	3	Cycle
		CL = 2		2	2	2	Cycle
7	Burst Stop Command to Output in High-Z Delay	CL = 3	l_{BSH}	3	3	3	Cycle
		CL = 2		2	2	2	Cycle
8	Mode Register Access to Bank Active (min)		l_{MRD}	2	2	2	Cycle
9	$\overline{CAS}$ to $\overline{CAS}$ Delay (min)		l_{CCD}	1	1	1	Cycle
10	$\overline{CAS}$ Bank Delay (min)		l_{CBD}	1	1	1	Cycle
11	Write to Precharge Read Delay	CL = 3	l_{RWL}	1	1	1	Cycle
		CL = 2		1	1	1	Cycle

Notes: *1. Assumes t_{RCD} and t_{CAC} are satisfied.
*2. t_{AC} also specifies the access time at burst mode except for first access.
*3. Specified where output buffer is no longer driven.
*4. Actual clock count of t_{RC} (l_{RC}) will be sum of clock count of t_{RAS} (l_{RAS}) and t_{RP} (l_{RP}).
*5. t_{RAC} is a reference value. Maximum value is obtained from the sum of t_{RCD} (min) and t_{CAC} (max).
*6. Assumes t_{RAC} and t_{AC} are satisfied.
*7. Operation within the t_{RCD} (min) ensures that t_{RAC} can be met; if t_{RCD} is greater than the specified t_{RCD} (min), access time is determined by t_{CAC} and t_{AC}.
*8. All base values are measured from the clock edge at the command input to the clock edge for the next command input.
All clock counts are calculated by a simple formula:
clock count equals base value divided by clock period (round off to a whole number).
*9. The l_{CAC} (CAS latency: CL) is programmed by the mode register.
*10. An initial pause (DESL on NOP) of 200 µs is required after power-up followed by a minimum of eight Auto-refresh cycles.
*11. 1.4 V or V_{REF} is the reference level for measuring timing of signals.
Transition times are measured between V_{IH} (min) and V_{IL} (max).
*12. AC characteristics assume t_T = 1 ns and 30 pF of capacitive load.

*Source: See MB811641642A Data Sheet for details on the electricals.

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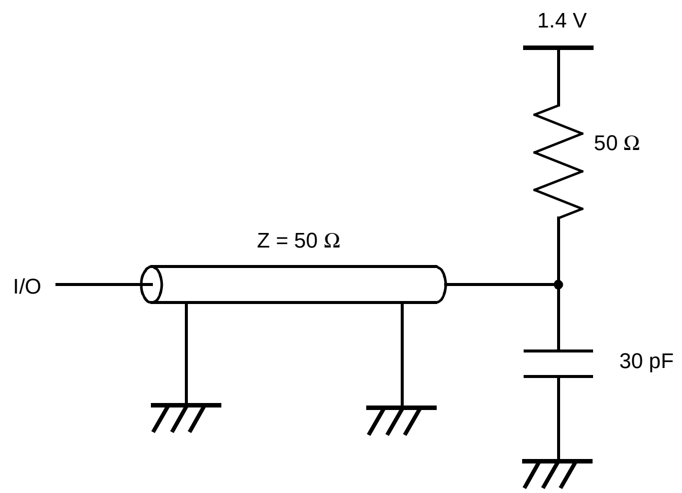
■ AC OPERATING TEST CONDITION (Example of AC Test Load Circuit)



MB8504S064AE-100/-84/-67/-100L/-84L/-67L

■ SERIAL PRESENCE DETECT(SPD) FUNCTION

1. PIN DESCRIPTIONS

SCL (Serial Clock)

SCL input is used to clock all data input/output of SPD

SDA (Serial Data)

SDA is a common pin used for all data input/output of SPD. The SDA pull-up resistor is required due to the open-drain output.

SA_0, SA_1, SA_2 (Address)

Address inputs are used to set the least significant three bits of the eight bits slave address. The address inputs must be fixed to select a particular module and the fixed address of each module must be different each other. For this module, any address inputs are not required because all addresses (SA_0, SA_1, SA_2) are driven to V_{SS} on the module.

2. SPD OPERATIONS

CLOCK and DATA CONVENTION

Data states on the SDA can change only during SCL = Low. SDA state changes during SCL = High are indicated start and stop conditions. Refer to Fig. 1 below.

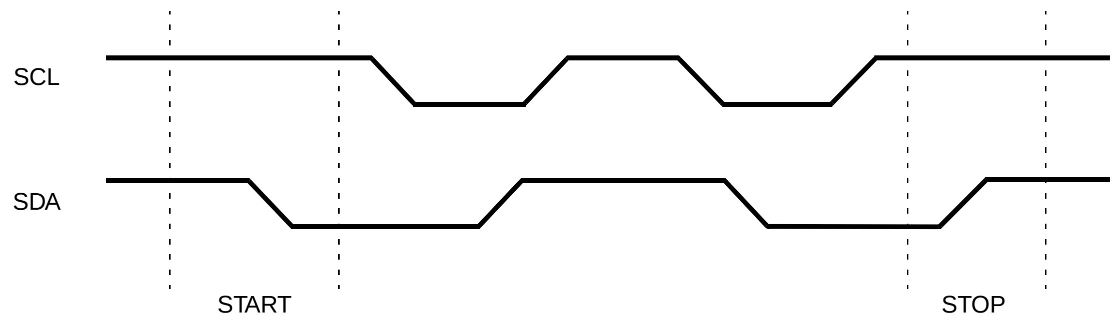
START CONDITION

All commands are preceded by a start condition, which is a transition of SDA state from High to Low when SCL = High. SPD will not respond to any command until this condition has been met.

STOP CONDITION

All read or write operation must be terminated by a stop condition, which is a transition of SDA state from Low to High when SCL = High. The stop condition is also used to make the SPD into the state of standby power mode after a read sequence.

Fig. 1 – START AND STOP CONDITIONS



START = High to Low transition of SDA state when SCL is High
STOP = Low to High transition of SDA state when SCL is High

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will put the SDA line to Low in order to acknowledge that it received the eight bits of data.

The SPD will respond with an acknowledge when it received the start condition followed by slave address issued by master.

In the read operation, the SPD will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is issued by master, the SPD will continue to transmit data. If an acknowledge is not detected, the SPD will terminated further data transmissions. The master must then issue a stop condition to return the SPD to the standby power mode.

In the write operation, upon receipt of eight bits of data the SPD will respond with an acknowledge, and await the next eight bits of data, again reponding with an acknowledge until the stop condition is issued by master.

SLAVE ADDRESS ADDRESSING

Following a start condition, the master must output the eight bits slave address. The most significant four bits of the slave address are device type identifier. For the SPD this is fixed as 1010[B]. Refer to the Fig. 2 below.

The next three significant bits are used to select a particular device. A system could have up to eight SPD devices —namely up to eight modules— on the bus. The eight addresses for eight SPD devices are defined by the state of the SA_0, SA_1 and SA_2 inputs. For this module, the three bits are fixed as 000[B] because all addresses are driven to V_{SS} on the module. Therefore, no address inputs are required.

The last bit of the slave address defines the operation to be performed. When $R/\overline{W}$ bit is "1", a read operation is selected, when $R/\overline{W}$ bit is "0", a write operation is selected.

Following the start condition, the SPD monitors the SDA line comparing the slave address being transmitted with its slave address (device type and state of SA_0, SA_1, and SA_2 inputs). Upon a correct compare the SPD outputs an acknowledge on the SDA line. Depending on the state of the $R/\overline{W}$ bit, the SPD will execute a read or write operation.

Fig. 2 – SLAVE ADDRESS

DEVICE TYPE IDENTIFIER				DEVICE ADDRESS			
1	0	1	0	SA_2	SA_1	SA_0	$R/\overline{W}$

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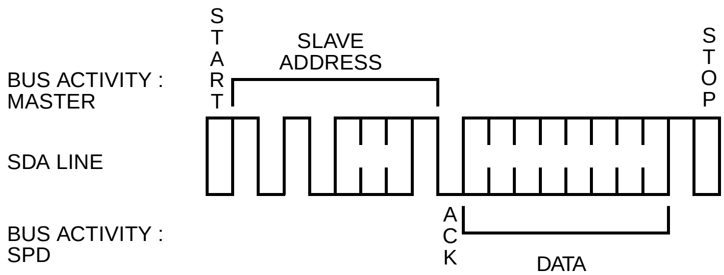
3. READ OPERATIONS

CURRENT ADDRESS READ

Internally the SPD contains an address counter that maintains the address of the last data accessed, incremented by one. Therefore, if the last access (either a read or write operation) was to address(n), the next read operation would access data from address(n+1). Upon receipt of the slave address with the R/$\overline{W}$ bit = "1", the SPD issues an acknowledge and transmits the eight bits of data during the next eight clock cycles. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig. 3 for the sequence of address, acknowledge and data transfer.

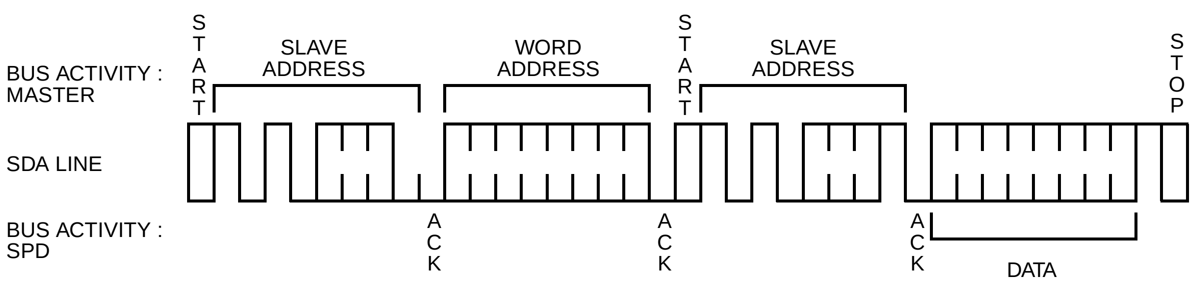
Fig. 3 – CURRENT ADDRESS READ



RANDOM READ

Random Read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit = "1", the master must first perform a "dummy" write operation on the SPD. The master issues the start condition, and the slave address followed by the word address. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit = "1". This will be followed by an acknowledge from the SPD and then by the eight bits of data. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig. 4 for the sequence of address, acknowledge and data transfer.

Fig. 4 – RANDOM READ

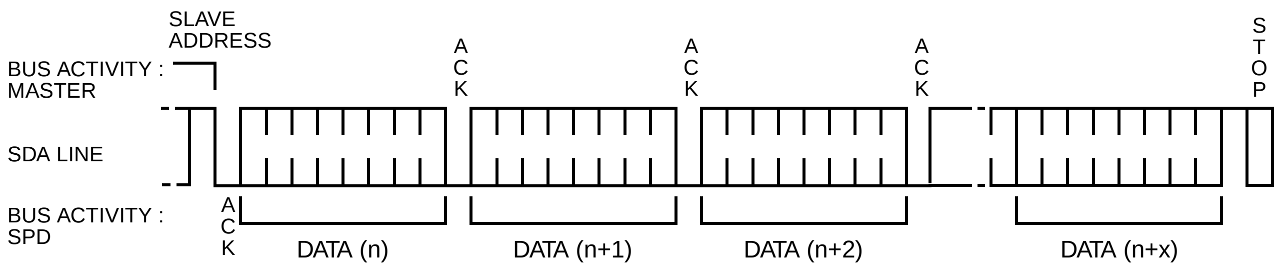


SEQUENTIAL READ

Sequential Read can be initiated as either a current address read or random read. The first data are transmitted as with the other read mode, however, the master now responds with an acknowledge, indicating it requires additional data. The SPD continues to output data for each acknowledge received. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig. 5 for the sequence of address, acknowledge and data transfer.

The data output is sequential, with the data from address(n) followed by the data from address(n+1). The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter “rolls over” to address0 and the SPD continues to output data for each acknowledge received.

Fig. 5 – SEQUENTIAL READ



4. DC CHARACTERISTICS

Parameter	Note	Symbol	Condition	Value		Unit
				Min.	Max.	
Input Leakage Current		S_{ILI}	$0\ V \leq V_{IN} \leq V_{CC}$	–10	10	µA
Output Leakage Current		S_{ILO}	$0\ V \leq V_{OUT} \leq V_{CC}$	–10	10	µA
Output Low Voltage	*1	S_{VOL}	I_{OL} = 3.0 mA	—	0.4	V

Note: *1. Referenced to V_{SS}.

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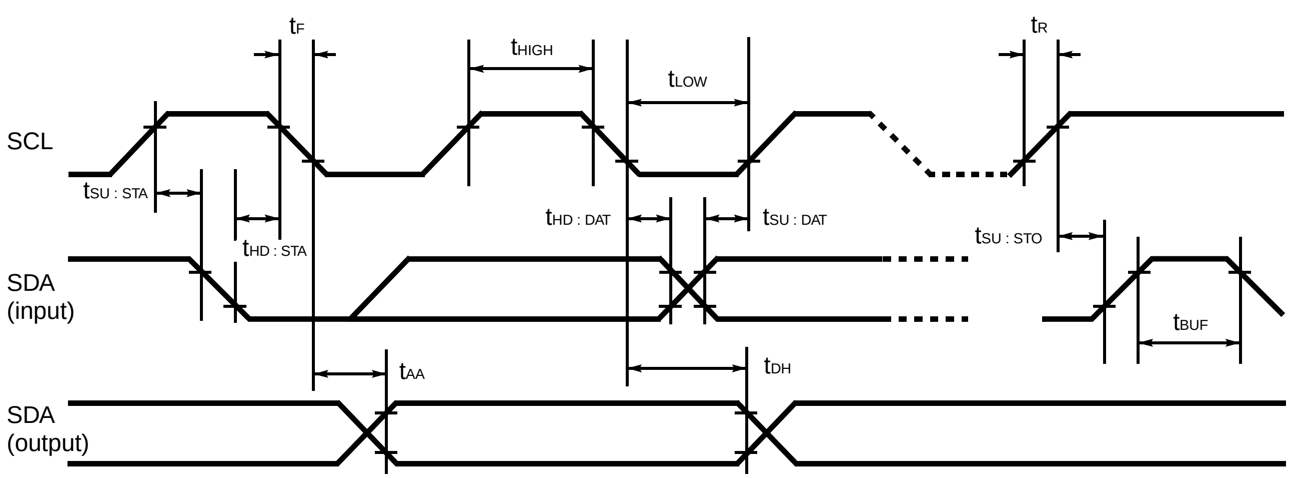
5. AC CHARACTERISTICS

No.	Parameter	Symbol	Value		Unit
			Min.	Max.	
1	SCL Clock Frequency	f_{SCL}	—	100	KHz
2	Noise Suppression Time Constant at SCL, SDA Inputs	T_I	—	100	ns
3	SCL Low to SDA Data Out Valid	t_{AA}	—	3.5	µs
4	Time the Bus Must Be Free Before a New Transmission Can Start	t_{BUF}	4.7	—	µs
5	Start Condition Hold Time	$t_{HD:STA}$	4.0	—	µs
6	Clock Low Period	t_{LOW}	4.7	—	µs
7	Clock High Period	t_{HIGH}	4.0	—	µs
8	Start Condition Setup Time	$t_{SU:STA}$	4.7	—	µs
9	Data in Hold Time	$t_{HD:DAT}$	0	—	µs
10	Data in Setup Time	$t_{SU:DAT}$	250	—	ns
11	SDA and SCL Rise Time	t_R	—	1	µs
12	SDA and SCL Fall Time	t_F	—	300	ns
13	Stop Condition Setup Time	$t_{SU:STO}$	4.7	—	µs
14	Data Out Hold Time	t_{DH}	100	—	ns
15	Write Cycle Time	t_{WR}	—	15	ms

Fig. 6 – TIMING WAVEFORM



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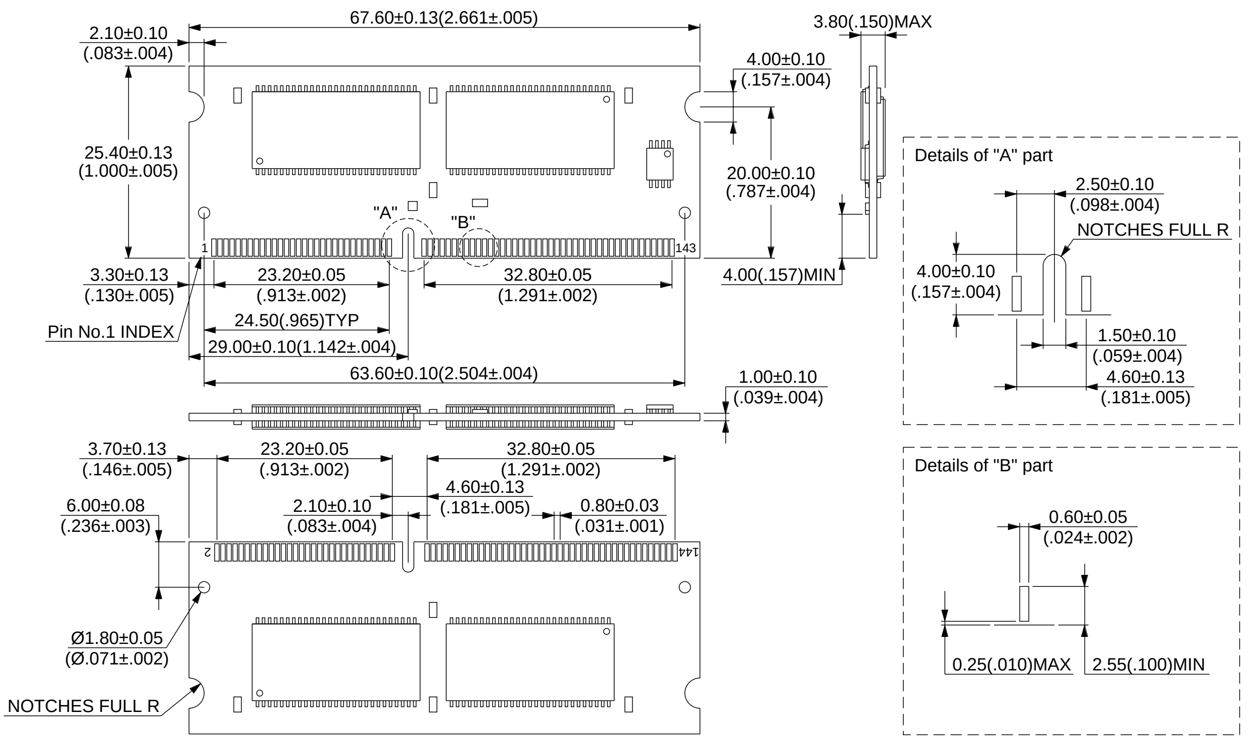
■ PACKAGE DIMENSION

144-pin plastic DIMM (socket type)
(MDS-144P-P08)



Dimension in mm (inches)

MB8504S064AE-100/-84/-67/-100L/-84L/-67L

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